OBSOLETE PRODUCT
RECOMMENDED REPLACEMENT PART
ISL36411

QLx411GRx

Quad Lane Extender

QLx411GRx

The QLx411GRx is a settable quad receive-side equalizer with extended functionality for advanced protocols operating with line rates up to 11.3Gb/s such as InfiniBand (SDR, DDR and QDR) and 40G Ethernet (40GBase-CR4). The QLx411GRx compensates for the frequency dependent attenuation of copper twin-axial cables, extending the signal reach up to at least 10m on 28AWG cable.

The small form factor, highly-integrated quad design is ideal for high-density data transmission applications including active copper cable assemblies. The four equalizing filters within the QLx411GRx can each be set to provide optimal signal fidelity for a given media and length. The compensation level for each filter is set by two external control pins.

Operating on a single 1.2V power supply, the QLx411GRx enables per channel throughputs of 10Gb/s to 11.3Gb/s while supporting lower data rates including 8.5, 6.25, 5, 4.25, 3.125, and 2.5Gb/s. The QLx411GRx uses current mode logic (CML) inputs/outputs and is packaged in a 4mmx7mm 46 lead QFN. Individual lane LOS support is included for module applications.

Features

- Supports data rates up to 11.3Gb/s
- Low power (135mW per channel)
- Low latency (<500ps)
- Four equalizers in a 4mmx7mm QFN package for straight route-through architecture and simplified routing
- Each equalizer boost is independently pin selectable
- Supports 64b/66b encoded data – long run lengths
- Line silence preservation
- 1.2V supply voltage
- Individual lane LOS support

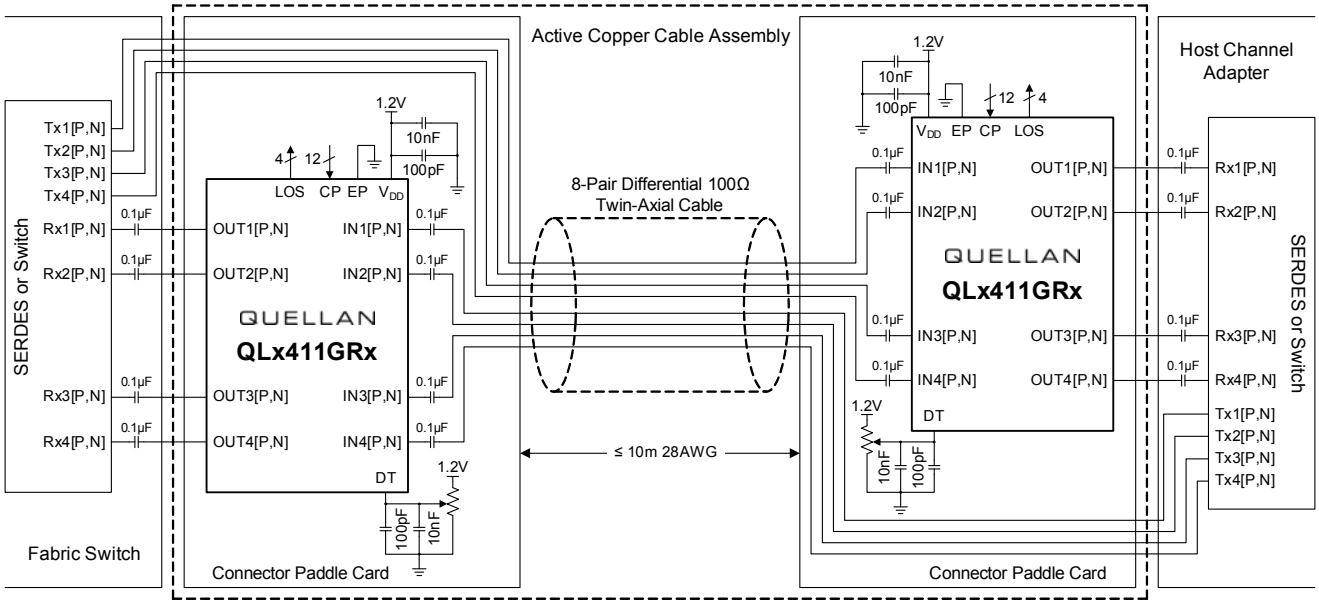
Applications

- QSFP active copper cable modules
- InfiniBand SDR, DDR and QDR
- 40G Ethernet (40GBase-CR4)
- XAUI and RXAUI
- High-speed active cable assemblies
- High-speed printed circuit board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

Typical Application Circuit



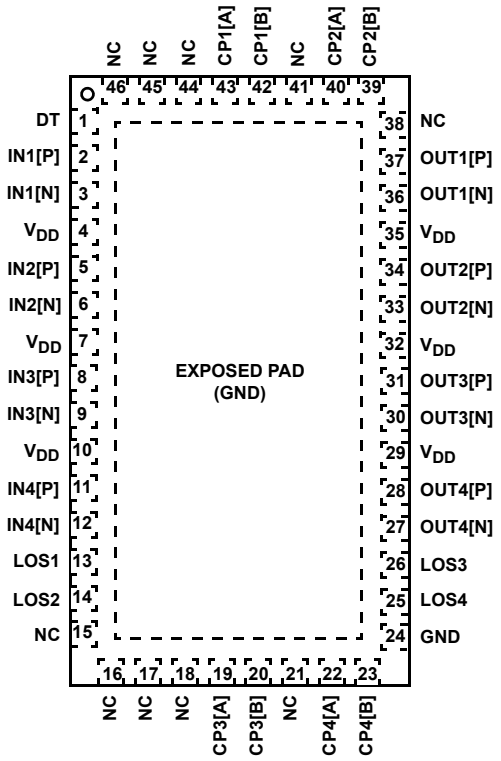
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
QLX411RIQT7	QLX411RIQ	0 to +70	46 Ld QFN 7” Prod. Tape & Reel; Qty 1,000	L46.4x7
QLX411RIQSR	QLX411RIQ	0 to +70	46 Ld QFN 7” Sample Reel; Qty 100	L46.4x7

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

QLx411GRx
(46 LD 4x7 QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
DT	1	Detection Threshold. Reference DC voltage threshold for input signal power detection. Data output OUT[k] is muted when the power of the equalized version of IN[k] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the limiting amplifier.
IN1[P,N]	2, 3	Equalizer 1 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
V_{DD}	4, 7, 10, 29, 32, 35	Power supply. 1.2V supply voltage. The use of parallel 100pF and 10nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN2[P,N]	5, 6	Equalizer 2 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
IN3[P,N]	8, 9	Equalizer 3 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
IN4[P,N]	11, 12	Equalizer 4 differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOS1	13	LOS indicator 1. High output when equalized IN1 signal is below DT threshold.
LOS2	14	LOS indicator 2. High output when equalized IN2 signal is below DT threshold.
NC	15, 16, 18, 21, 38, 41, 44, 45, 46	Not connected: Do not make any connections to these pins.
CP3[A,B,]	19, 20	Control pins for setting equalizer 3. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP4[A,B,]	22, 23	Control pins for setting equalizer 4. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
GND	24	This pin should be grounded.
LOS4	25	LOS indicator 4. High output when equalized IN1 signal is below DT threshold.
LOS3	26	LOS indicator 3. High output when equalized IN2 signal is below DT threshold.
OUT4[N,P]	27, 28	Equalizer 4 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT3[N,P]	30, 31	Equalizer 3 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT2[N,P]	33, 34	Equalizer 2 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
OUT1[N,P]	36, 37	Equalizer 1 differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
CP2[B,A]	39, 40	Control pins for setting equalizer 2. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
CP1[B,A]	42, 43	Control pins for setting equalizer 1. CMOS logic inputs. Pins are read as a 3-digit number to set the boost level. A is the MSB, and B is the LSB. Pins are internally pulled down through a 25kΩ resistor.
EXPOSED PAD	-	Exposed ground pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.3V
Voltage at All Input Pins . . . . . -0.3V to V_{DD} + 0.3V
ESD Rating at All Pins . . . . . 2kV (HBM)

Thermal Information

Operating Ambient Temperature Range . . . . . 0°C to +70°C
Storage Ambient Temperature Range . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	70	°C
Bit Rate		NRZ data applied to any channel	2.5		11.3	Gb/s

Control Pin Characteristics

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output LOW Logic Level	V_{OL}	LOS[k]	0	0	250	mV
Output HIGH Logic Level	V_{OH}	LOS[k]	1000		V_{DD}	mV
Input Current		Current draw on digital pin, i.e., CP[k][A,B]		30	100	µA

Electrical Specifications

Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}			360		mA	
Cable Input Amplitude Range	V_{IN}	Measured differentially at data source before encountering channel loss	600	1200	1600	mV_{P-P}	1
DC Differential Input Resistance		Measured on input channel IN[k]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[k]P or IN[k]N	40	50	60	Ω	
Input Return Loss (Differential)	$S_{DD}11$	100MHz to 7.5GHz	8			dB	2
Input Return Loss (Common Mode)	$S_{CC}11$	100MHz to 7.5GHz	8			dB	2
Input Return Loss (Com. to Diff. Conversion)	$S_{DC}11$	100MHz to 7.5GHz	20			dB	2
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[k]P and OUT[k]N with 50Ω load on both output pins	450	600	650	mV_{P-P}	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss (Differential)	$S_{DD}22$	100MHz to 7.5GHz	8			dB	2
Output Return Loss (Common Mode)	$S_{CC}22$	100MHz to 7.5GHz	8			dB	2
Output Return Loss (Com. to Diff. Conversion)	$S_{DC}22$	100MHz to 7.5GHz	20			dB	2

Electrical Specifications Typical values are at V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. V_{DD} = 1.1V to 1.3V, T_A = 0°C to +70°C. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Residual Jitter		10Gb/s; Up to 10m 28AWG standard twin-axial cable (approx. -27dB @ 5GHz); 1200mV_{P-P} ≤ VIN ≤ 1600mV_{P-P}		0.25		UI	1, 3, 4
Output Transition Time	t_r, t_f	20% to 80%		35		ps	5
Lane-to-Lane Skew					50	ps	
Propagation Delay		From IN[k] to OUT[k]			500	ps	
LOS Assert Time		Time to assert Loss-of-Signal (LOS) indicator when transitioning from active data mode to line silence mode			50	µs	6
LOS De-Assert Time		Time to de-assert Loss-of-Signal (LOS) indicator when transitioning from line silence mode to active data mode			50	µs	6
Data-to-Line Silence Response Time		Time to transition from active data to line silence (muted output) on 20m 28AWG standard twin-axial cable at 5Gb/s			50	µs	6
Line Silence-to-Data Response Time		Time to transition from line silence mode (muted output) to active data on 20m 28AWG standard twin-axial cable at 5Gb/s			50	µs	6

NOTES:

1. After channel loss, differential amplitudes at QLx411GRx inputs must meet the input voltage range specified in “Absolute Maximum Ratings” on page 4.
2. Temperature = +25°C, V_{DD} = 1.2V.
3. Output residual jitter is the difference between the total jitter at the lane extender output and the total jitter of the transmitted signal (as measured at the input to the channel). Total jitter (TJ) is DJ_{pp} + 14.1 x RJ_{RMS}.
4. Measured using a PRBS 2^7-1 pattern. Deterministic jitter at the input to the lane extender is due to frequency-dependent, media-induced loss only.
5. Rise and fall times measured using a 1GHz clock with a 20ps edge rate.
6. For active data mode, cable input amplitude is 300mV_{P-P} (differential) or greater. For line silence mode, cable input amplitude is 20mV_{P-P} (differential) or less.

Typical Performance Characteristics

Performance is measured using the test setup illustrated in Figure 1. The signal from the pattern generator is launched into the twin-ax cable using an SMA/CX4 adapter card. The chip evaluation board is connected to the output of the cable through another adapter card. The QLx411GRx output signal is then visualized on a scope to determine signal integrity parameters such as jitter (Note 7).

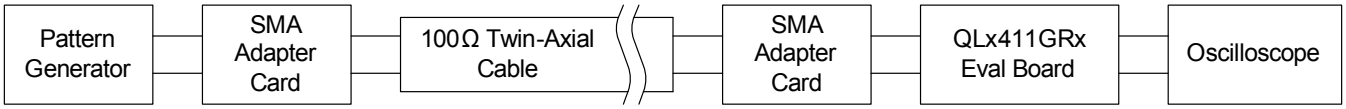


FIGURE 1. DEVICE CHARACTERIZATION SET UP

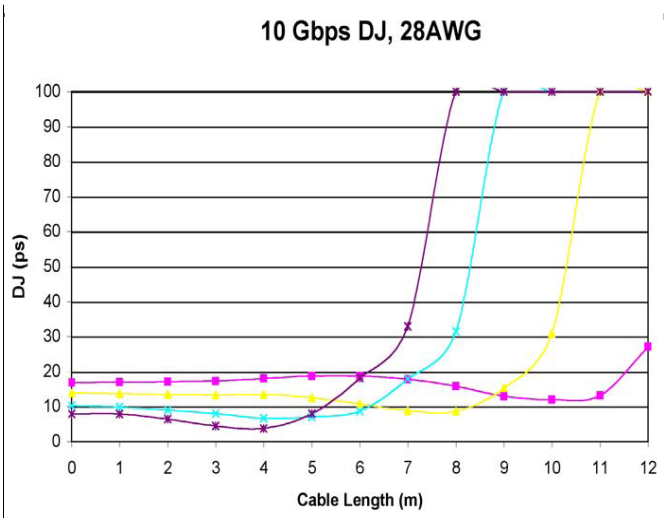


FIGURE 2. JITTER vs CABLE LENGTH AT 10Gb/s (BOOST LEVELS 0-3)

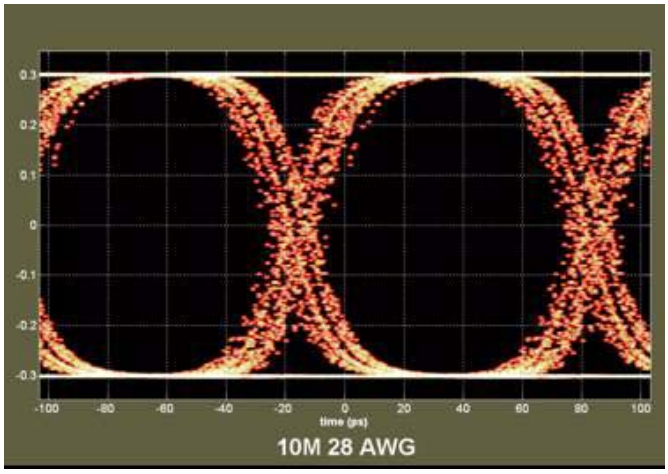


FIGURE 3. QLx411GRx 10Gb/s OUTPUT FOR A 10M 28AWG CABLE

NOTE:

7. Prior to the tapeout, the data in Figures 2 and 3 represents simulations approximating the conditions of setup in Figure 1, not measured data.

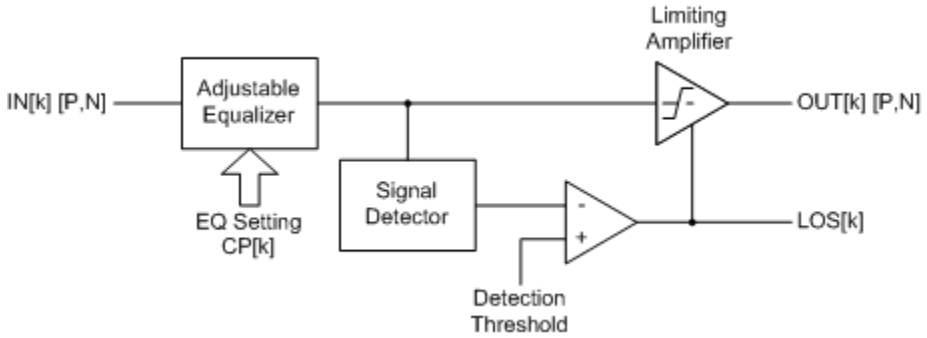


FIGURE 4. FUNCTIONAL DIAGRAM OF A SINGLE CHANNEL WITHIN THE QLx411GRx

Operation

The QLx411GRx is an advanced quad lane-extender for high-speed interconnects. A functional diagram of one of the four channels in the QLx411GRx is shown in Figure 4. In addition to a robust equalization filter to compensate for channel loss and restore signal fidelity, the QLx411GRx contains unique integrated features to preserve special signaling protocols typically broken by other equalizers. The signal detect function is used to mute the channel output when the equalized signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence ("quiescent state" in InfiniBand contexts). Furthermore, the output of the signal detect/DT comparator is used as a loss of signal (LOS) indicator to indicate the absence of a received signal.

As illustrated in Figure 4, the core of each high-speed signal path in the QLx411GRx is a sophisticated equalizer followed by a limiting amplifier. The equalizer compensates for skin loss, dielectric loss, and impedance discontinuities in the transmission channel. Each equalizer is followed by a limiting amplification stage that provides a clean output signal with full amplitude swing and fast rise-fall times for reliable signal decoding in a subsequent receiver.

Individually Adjustable Equalization Boost

Each channel in the QLx411GRx features an independently settable equalizer for custom signal restoration. The flexibility of this adjustable compensation architecture enables signal fidelity to be optimized on a channel-by-channel basis, providing support for a wide variety of channel characteristics and data rates ranging from 2.5Gb/s to 11.3Gb/s. Because the boost level is externally set rather than internally adapted, the QLx411GRx provides reliable communication from the very first bit transmitted. There is no time needed for adaptation and control loop convergence. Furthermore, there are no pathological data patterns that will cause the QLx411GRx to move to an incorrect boost level.

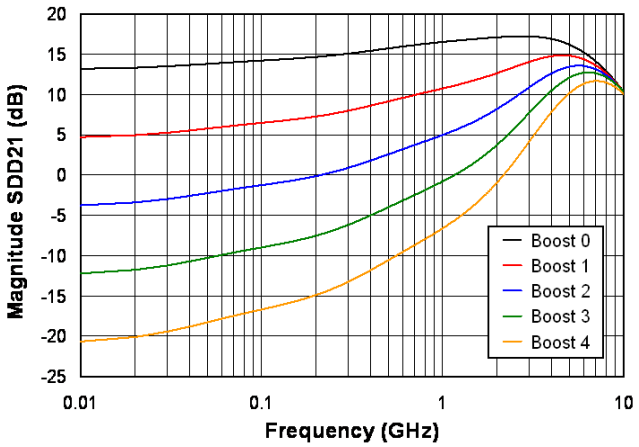


FIGURE 5. GAIN PROFILE FOR VARIOUS BOOST SETTINGS IN QLx411GRx

Control Pin Boost Setting

The connectivity of the CP pins is used to determine the boost level of each channel. Table 1 defines the mapping from the 2-bit CP word to the 5 possible boost levels.

TABLE 1. MAPPING BETWEEN BOOST LEVEL AND CP-PIN CONNECTIVITY

CP[A]	CP[B]	BOOST LEVEL
25kΩ	25kΩ	0
25kΩ	Open	1
25kΩ	0Ω	2
Open	25kΩ	3
Open	Open	4

CML Input and Output Buffers

The input and output buffers for the high-speed data channels in the QLx411GRx are implemented using CML. Equivalent input and output circuits are shown in Figures 6 and 7.

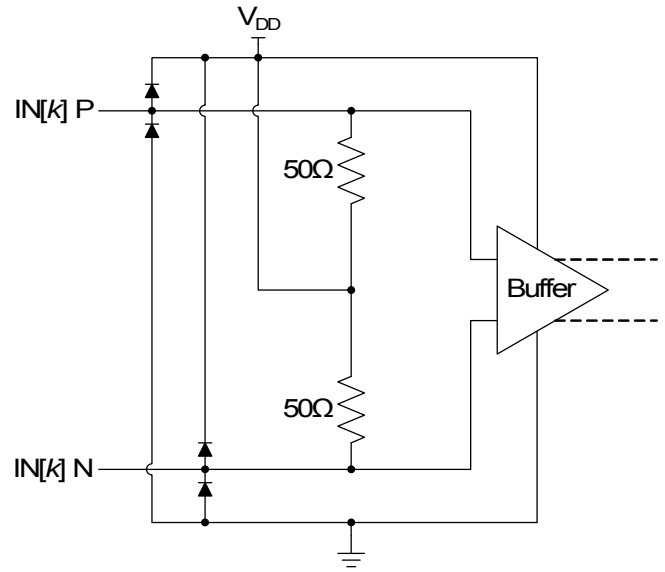


FIGURE 6. CML INPUT EQUIVALENT CIRCUIT FOR THE QLx411GRx

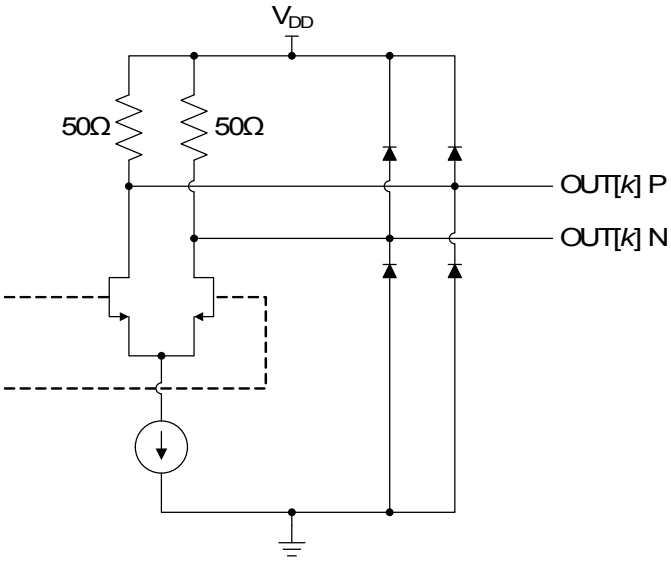


FIGURE 7. CML OUTPUT EQUIVALENT CIRCUIT FOR THE QLx411GRx

Line Silence / Quiescent Mode

Line silence is commonly broken by the limiting amplification in other equalizers. This disruption can be detrimental in many systems that rely on line silence as part of the protocol. The QLx411GRx contains special lane management capabilities to detect and preserve periods of line silence while still providing the fidelity-enhancing benefits of limiting amplification during active data transmission. Line silence is detected by measuring the amplitude of the equalized signal and comparing that to a threshold set by the voltage at the DT pin. When the amplitude falls below the threshold, the output driver stages are muted and held at their nominal common mode voltage[1].

LOS Indicator

Pins LOS[k] are used to output the state of the muting circuitry to serve as a loss of signal indicator for channel k. This signal is directly derived from the muting signal off the DT-threshold signal detector output. The LOS signal goes HIGH when the power signal is below the DT threshold and LOW when the power goes above the DT threshold. This feature is meant to be used in optical systems (e.g. QSFP) where there are no quiescent or electrical-idle states. In these cases, the DT threshold is used to determine the sensitivity of the LOS indicator.

1. The output common mode voltage remains constant during both active data transmission and output muting modes

Typical Application Reference Design

Figure 8 shows reference design schematics for a QLx411GRx evaluation board with an SMA connector interface.

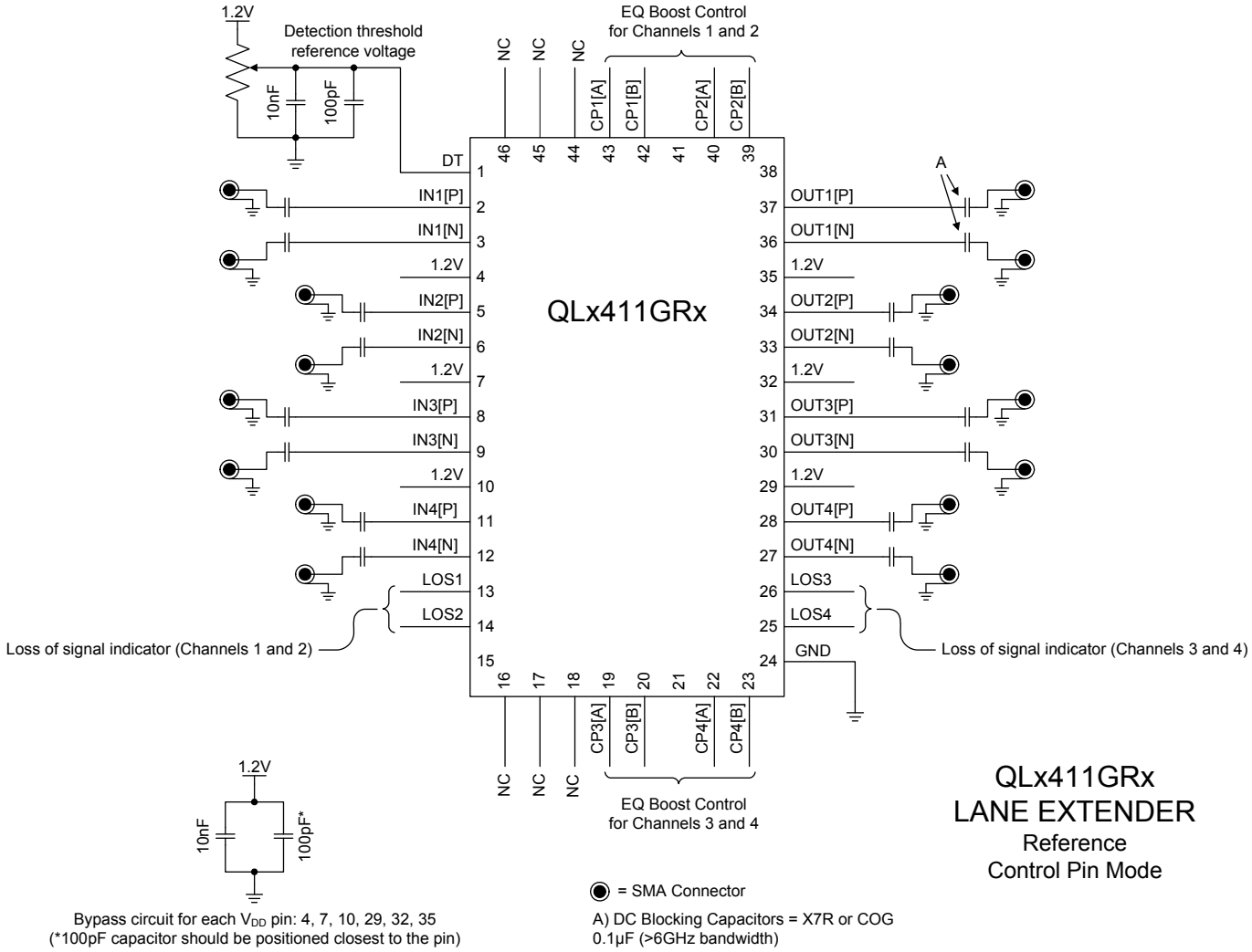


FIGURE 8. APPLICATION CIRCUIT FOR THE QLx411GRx EVALUATION BOARD SHOWING THE USE OF THE CONTROL PINS FOR SETTING THE EQUALIZER COMPENSATION LEVEL

About Q:ACTIVE®

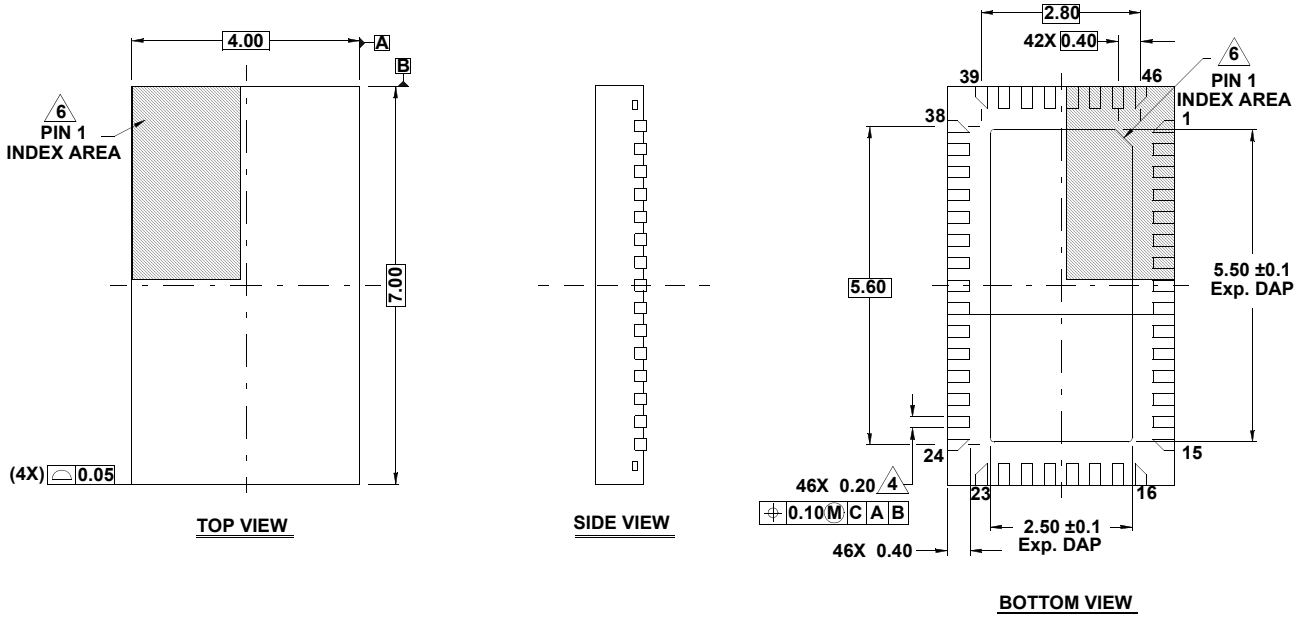
Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

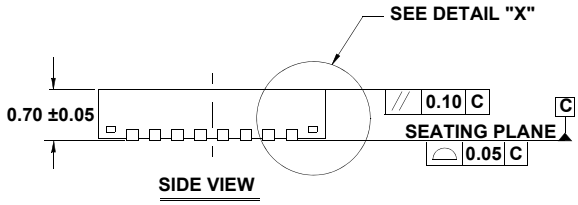
Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

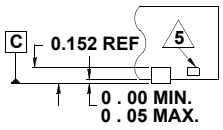
Package Outline Drawing

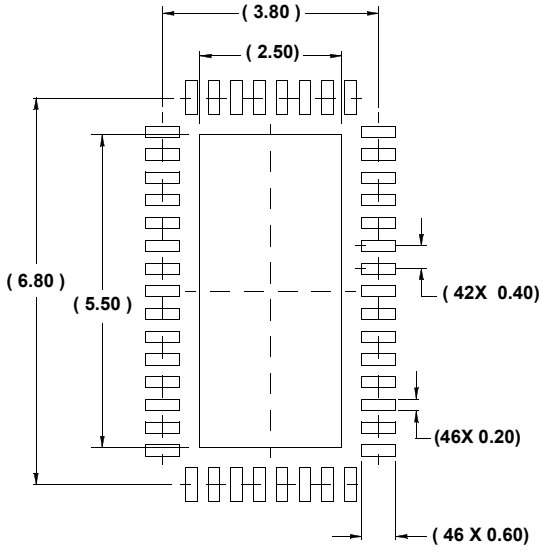
L46.4x7

46 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (TQFN)
Rev 0, 9/09









NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.